# Self-Protected Low Side Driver with Temperature and Current Limit

NCV8401 is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

#### **Features**

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- Over Voltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- RoHs Compliant
- AEC-Q101 Qualified
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- This is a Pb-Free Device

#### **Typical Applications**

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

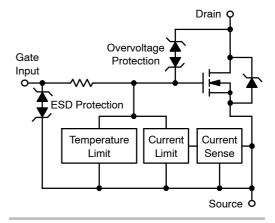


## ON Semiconductor®

#### http://onsemi.com

V <sub>DSS</sub> (Clamped)	R <sub>DS(ON)</sub> TYP	I <sub>D</sub> MAX (Limited)
42 V	23 m $\Omega$ @ 10 V	33 A*

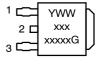
\*Max current may be limited below this value depending on input conditions.





## MARKING DIAGRAM

#### DPAK CASE 369C STYLE 2



Y = Year

WW = Work Week 1 = Gate
xxx = Device Code 2 = Drain
G = Pb-Free Package 3 = Source

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NCV8401DTRKG	DPAK (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	$V_{DSS}$	42	V
Drain-to-Gate Voltage Internally Clamped ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{\mathrm{DGR}}$	42	V
Gate-to-Source Voltage	V <sub>GS</sub>	±14	V
Drain Current - Continuous		Internally Limited	
Total Power Dissipation @ $T_A = 25^{\circ}C$ (Note 1) @ $T_A = 25^{\circ}C$ (Note 2)	P <sub>D</sub>	1.1 2.0	W
Thermal Resistance,  Junction-to-Case  Junction-to-Ambient (Note 1)  Junction-to-Ambient (Note 2)	$R_{ heta JC} \ R_{ heta JA} \ R_{ heta JA}$	1.6 110 60	°C/W
Single Pulse Drain–to–Source Avalanche Energy ( $V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, $I_L$ = 3.65 Apk, $L$ = 120 mH, $R_G$ = 25 $\Omega$ , $T_{Jstart}$ = 150°C) (Note 3)		800	mJ
Load Dump Voltage (V <sub>GS</sub> = 0 and 10 V, R <sub>I</sub> = 2.0 $\Omega$ , R <sub>L</sub> = 3.0 $\Omega$ , t <sub>d</sub> = 400 ms)		65	V
Operating Junction Temperature		-40 to 150	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Minimum FR4 PCB, steady state.
- 2. Mounted onto a 2" square FR4 board (1" square, 2 oz. Cu 0.06" thick single-sided, t = steady state).
- 3. Not subject to production testing.

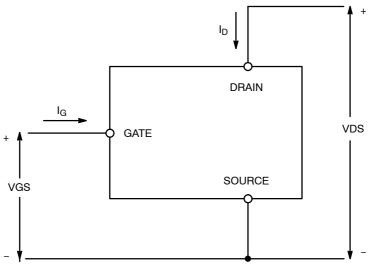


Figure 1. Voltage and Current Convention

## $\textbf{MOSFET ELECTRICAL CHARACTERISTICS} \ (T_J = 25^{\circ}\text{C unless otherwise noted})$

Characte	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS					1	ı
Drain-to-Source Clamped Breakdown Vo $(V_{GS}=0~Vdc,~I_D=250~\mu Adc)$ $(V_{GS}=0~Vdc,~I_D=250~\mu Adc,~T$	V <sub>(BR)DSS</sub>	42 42	46 44	50 50	Vdc	
Zero Gate Voltage Drain Current $(V_{DS} = 32 \text{ Vdc}, V_{GS} = 0 \text{ Vdc})$ $(V_{DS} = 32 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, T_{GS} = 0 \text{ Vdc})$	I <sub>DSS</sub>		1.5 6.5	5.0	μAdc	
Gate Input Current (V <sub>GS</sub> = 5.0 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSSF</sub>		50	100	μAdc	
ON CHARACTERISTICS						
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = 1.2 \text{ mAdc})$ Threshold Temperature Coeffic	V <sub>GS(th)</sub>	1.0	1.8 5.0	2.0	Vdc -mV/°C	
Static Drain-to-Source On-Resistance ( $V_{GS} = 10 \text{ Vdc}$ , $I_D = 5.0 \text{ Adc}$ , $T_C = 10 \text{ Vdc}$ , $I_D = 5.0 \text{ Adc}$ , $T_C = 10 \text{ Vdc}$ , $T_C = 10 \text{ Vdc}$ , $T_C = 10 \text{ Vdc}$	R <sub>DS(on)</sub>		23 43	29 55	mΩ	
Static Drain-to-Source On-Resistance (I $(V_{GS} = 5.0 \text{ Vdc}, I_D = 5.0 \text{ Adc}, T $ $(V_{GS} = 5.0 \text{ Vdc}, I_D = 5.0 \text{ Adc}, T $	R <sub>DS(on)</sub>		28 50	34 60	mΩ	
Source-Drain Forward On Voltage $(I_S = 5 \text{ A}, V_{GS} = 0 \text{ V})$	V <sub>SD</sub>		0.80	1.1	V	
SWITCHING CHARACTERISTICS (Note	4)					
Turn-ON Time (10% V <sub>IN</sub> to 90% I <sub>D</sub> )	V <sub>IN</sub> = 0 V to 5 V, V <sub>DD</sub> = 25 V	t <sub>ON</sub>		41	50	μs
Turn-OFF Time (90% V <sub>IN</sub> to 10% I <sub>D</sub> )	$I_D = 1.0 \text{ A, Ext } R_G = 2.5 \Omega$	t <sub>OFF</sub>		129	150	
Turn-ON Time (10% V <sub>IN</sub> to 90% I <sub>D</sub> )	V <sub>IN</sub> = 0 V to 10 V, V <sub>DD</sub> = 25 V	t <sub>ON</sub>		16	25	
Turn-OFF Time (90% V <sub>IN</sub> to 10% I <sub>D</sub> )	$I_D = 1.0 \text{ A}, \text{ Ext } R_G = 2.5 \Omega$	t <sub>OFF</sub>		164	180	
Slew-Rate ON (20% V <sub>DS</sub> to 50% V <sub>DS</sub> )	V <sub>in</sub> = 0 to 10 V, V <sub>DD</sub> = 12 V,	-dV <sub>DS</sub> /dt <sub>ON</sub>		1.27		V/μs
Slew-Rate OFF (80% V <sub>DS</sub> to 50% V <sub>DS</sub> )	$V_{in}$ = 0 to 10 V, $V_{DD}$ = 12 V, $R_L$ = 4.7 $\Omega$	dV <sub>DS</sub> /dt <sub>OFF</sub>		0.36		
SELF PROTECTION CHARACTERISTIC	S (T <sub>J</sub> = 25°C unless otherwise noted)	•				
Current Limit	$V_{GS} = 5.0 \text{ V}, V_{DS} = 10 \text{ V}$ $V_{GS} = 5.0 \text{ V}, T_J = 150^{\circ}\text{C}$ (Note 4)	I <sub>LIM</sub>	25 11	30 16	35 21	Adc
	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 10 V V <sub>GS</sub> = 10 V, T <sub>J</sub> = 150°C (Note 4)		30 18	35 25	40 28	
Temperature Limit (Turn-off)	V <sub>GS</sub> = 5.0 V (Note 4)	$T_{LIM(off)}$	150	175	200	°C
Thermal Hysteresis	V <sub>GS</sub> = 5.0 V	$\Delta T_{LIM(on)}$		15		°C
Temperature Limit (Turn-off)	V <sub>GS</sub> = 10 V (Note 4)	$T_{LIM(off)}$	150	165	185	°C
Thermal Hysteresis	V <sub>GS</sub> = 10 V	$\Delta T_{LIM(on)}$		15		°C
GATE INPUT CHARACTERISTICS (Note	<del>2</del> 4)					
Device ON Gate Input Current	$V_{GS} = 5 \text{ V I}_{D} = 1.0 \text{ A}$	I <sub>GON</sub>		50		μΑ
	V <sub>GS</sub> = 10 V I <sub>D</sub> = 1.0 A			400		
Current Limit Gate Input Current	V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 10 V	I <sub>GCL</sub>		0.1		mA
	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 10 V			0.7		
Thermal Limit Fault Gate Input Current	$V_{GS} = 5 \text{ V}, V_{DS} = 10 \text{ V}$	I <sub>GTL</sub>		0.6		mA
	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 10 V			2.0		
ESD ELECTRICAL CHARACTERISTICS	(N <sub>J</sub> = 25°C unless otherwise noted) (N	lote 4)				
Electro-Static Discharge Capability Human Body Model (HBM) Machine Model (MM)		ESD	4000 400			V

<sup>4.</sup> Not subject to production testing.
5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

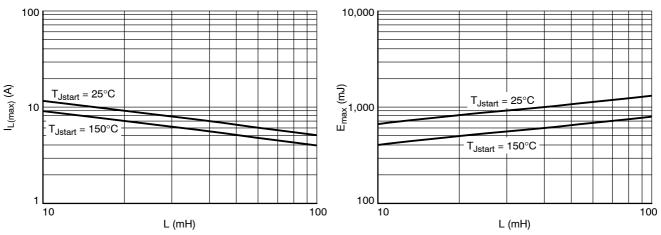


Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance

Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance

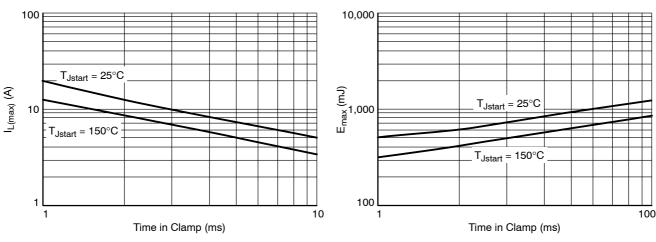


Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

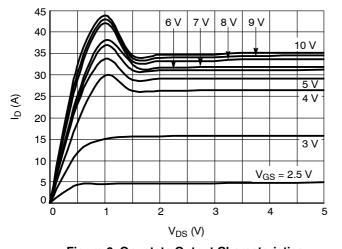


Figure 6. On-state Output Characteristics at 25°C

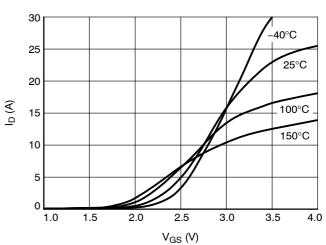
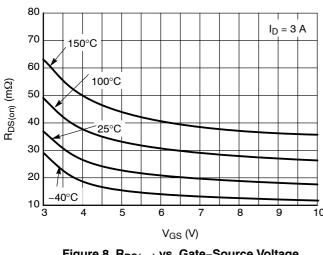


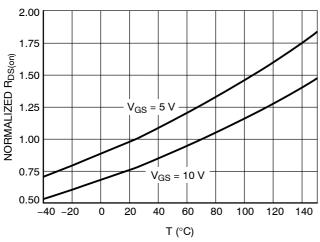
Figure 7. Transfer Characteristics (V<sub>DS</sub> = 10 V)



 $150^{\circ}C$ ,  $V_{GS} = 5 V$ 40  $150^{\circ}$ C,  $V_{GS} = 10 \text{ V}$ 35 R<sub>DS(on)</sub> (mΩ)  $100^{\circ}$ C,  $V_{GS} = 5$  V 30 25  $100^{\circ}C, V_{GS} = 10 V$ 25°C, V<sub>GS</sub> = 5 V 20 25°C, V<sub>GS</sub> = 10 V 15 -40°C, V<sub>GS</sub> = 5 V -40°C, V<sub>GS</sub> = 10 V 10 I<sub>D</sub> (A)

Figure 8. R<sub>DS(on)</sub> vs. Gate-Source Voltage

Figure 9. R<sub>DS(on)</sub> vs. Drain Current



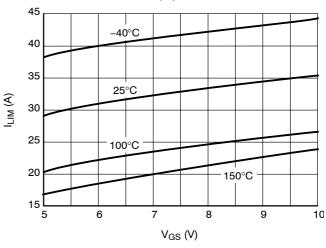
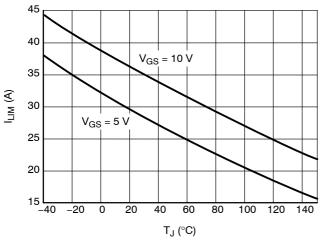


Figure 10. Normalized R<sub>DS(on)</sub> vs. Temperature  $(I_D = 5 \text{ A})$ 

Figure 11. Current Limit vs. Gate-Source Voltage (V<sub>DS</sub> = 10 V)



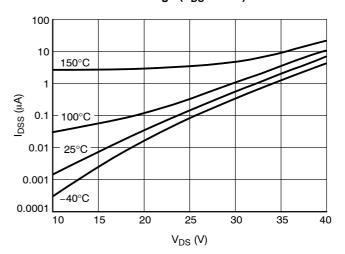
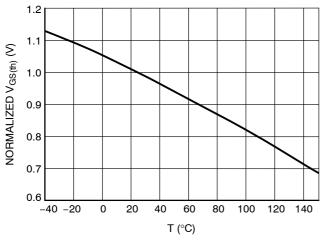


Figure 12. Current Limit vs. Junction Temperature (V<sub>DS</sub> = 10 V)

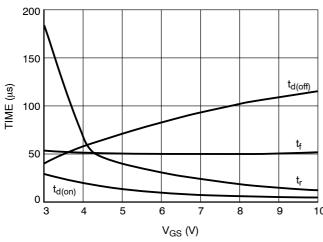
Figure 13. Drain-to-Source Leakage Current  $(V_{GS} = 0 V)$ 



1.0 0.9 -40°C 0.8 25°C V<sub>SD</sub> (V) 0.7 100°C 0.6 150°C 0.5 0.4 2 3 5 6 8 9 10 I<sub>S</sub> (A)

Figure 14. Normalized Threshold Voltage vs. Temperature ( $I_D = 1.2 \text{ mA}, V_{DS} = V_{GS}$ )

Figure 15. Source-Drain Diode Forward Characteristics (V<sub>GS</sub> = 0 V)



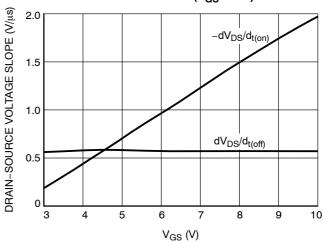
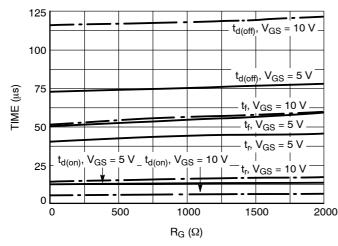


Figure 16. Resistive Load Switching Time vs. Gate–Source Voltage ( $V_{DD}$  = 25 V,  $I_{D}$  = 5 A,  $R_{G}$  = 0  $\Omega$ )

Figure 17. Resistive Load Switching Drain–Source Voltage Slope vs. Gate–Source Voltage ( $V_{DD}$  = 25 V,  $I_{D}$  = 5 A,  $R_{G}$  = 0  $\Omega$ )



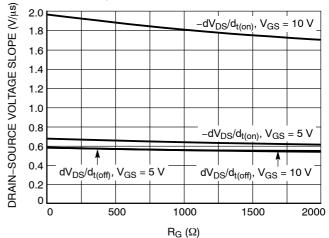


Figure 18. Resistive Load Switching Time vs. Gate Resistance ( $V_{DD} = 25 \text{ V}$ ,  $I_D = 5 \text{ A}$ )

Figure 19. Drain–Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance ( $V_{DD} = 25 \text{ V}, I_D = 5 \text{ A}$ )

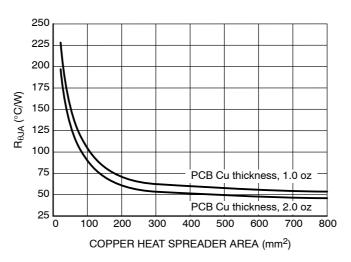


Figure 20.  $R_{\theta JA}$  vs. Copper Area

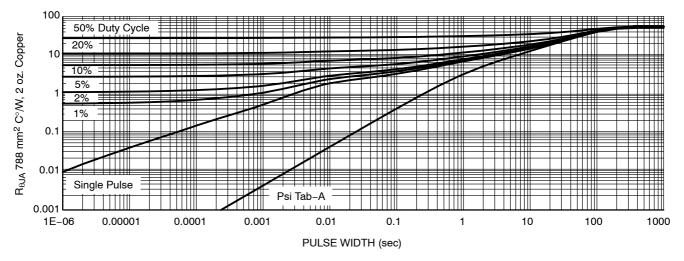


Figure 21. Transient Thermal Resistance

## **TEST CIRCUITS AND WAVEFORMS**

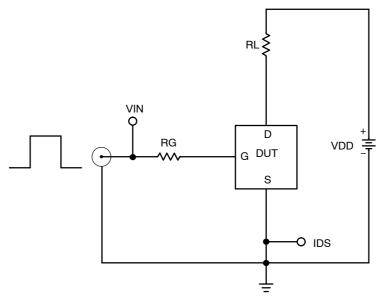


Figure 22. Resistive Load Switching Test Circuit

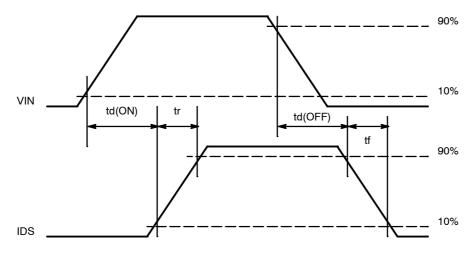


Figure 23. Resistive Load Switching Waveforms

## **TEST CIRCUITS AND WAVEFORMS**

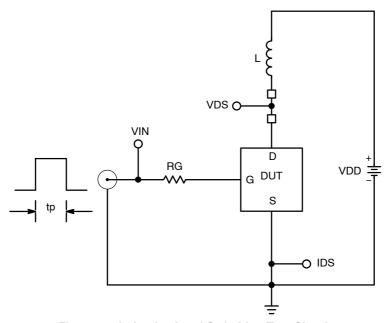


Figure 24. Inductive Load Switching Test Circuit

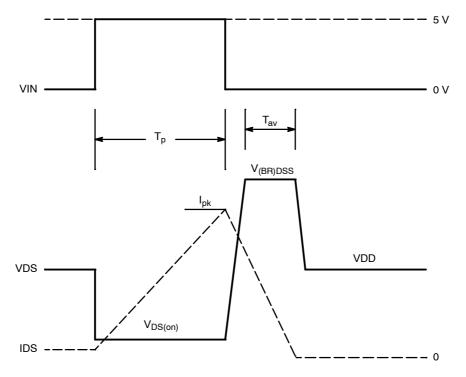
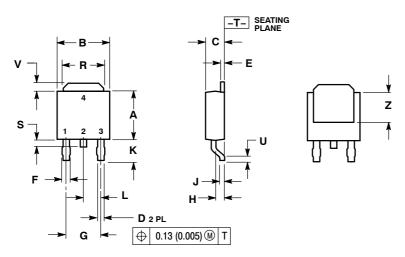


Figure 25. Inductive Load Switching Waveforms

#### PACKAGE DIMENSIONS

#### **DPAK**

CASE 369C-01 **ISSUE 0** 



#### NOTES:

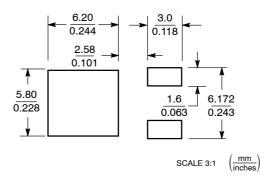
- 1. DIMENSIONING AND TOLERANCING
- PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.22
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020		0.51	
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

# STYLE 2: PIN 1. GATE

- 2. DRAIN 3. SOURCE
- 4. DRAIN

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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